5.1 Device Structure and Physical Operation

5.1.1 Device Structure

Typically $L = 0.1$ to $3 \, \mu m$, $W = 0.2$ to $100 \, \mu m$, and the thickness of the oxide layer ($t_{ox}$) is in the range of $2$ to $50 \, nm$. 

Figure 4.1  Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross-section. Typically $L = 0.1$ to $3 \, \mu m$, $W = 0.2$ to $100 \, \mu m$, and the thickness of the oxide layer ($t_{ox}$) is in the range of $2$ to $50 \, nm$. 

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5.2 Current-Voltage Characteristics

5.2.2 The $i_D$-$v_{DS}$ Characteristics (cont.)

Cut off region

$$v_{GS} < V_t$$

$$i_G = 0$$

$$i_D = 0$$
5.2 Current-Voltage Characteristics

5.2.2 The $i_D-v_{DS}$ Characteristics (cont.)

**Triode region**

\[ v_{GS} > V_t, \text{ and } v_{GD} > V_t \implies v_{GS} - v_{DS} > V_t \]

\[ i_D = k_n \frac{W}{L} \left[ (v_{GS} - V_t)v_{DS} - \frac{1}{2} v_{DS}^2 \right] \]

\[ \approx k_n \frac{W}{L} (v_{GS} - V_t)v_{DS} \quad (\text{If } v_{DS} \text{ is small}) \]

\[ r_{DS} = \left[ k_n \frac{W}{L} (v_{GS} - V_t) \right]^{-1} = \frac{1}{k_n} \frac{W}{L} V_{OV} \]

\[ V_{OV} = V_{GS} - V_t \]
5.2 Current-Voltage Characteristics

5.2.2 The $i_D - v_{DS}$ Characteristics (cont.)

**Saturation region**

$v_{GS} > V_t$, and $v_{GD} < V_t \Rightarrow v_{GS} - v_{DS} < V_t$

$$i_D = \frac{1}{2} k_n \frac{W}{L} \left( v_{GS} - V_t \right)^2$$

$$= \frac{1}{2} k_n \frac{W}{L} v_{DS}^2 \quad \text{(at the boundary)}$$
5.2 Current-Voltage Characteristics

5.2.2 The $i_D$-$v_{DS}$ Characteristics (cont.)

Saturation region

\[ v_{GS} > V_t, \text{ and } v_{GD} < V_t \Rightarrow v_{GS} - v_{DS} < V_t \]

\[
\begin{align*}
    i_D &= \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_t)^2 \\
    &= \frac{1}{2} k'_n \frac{W}{L} v_{DS}^2 \quad \text{(at the boundary)}
\end{align*}
\]

Figure 4.12 The $i_D$-$v_{GS}$ characteristic for an enhancement-type NMOS transistor in saturation ($V_t = 1$ V, $k'_n W/L = 1.0$ mA/V$^2$).
Example 5.3

Design the circuit so that the transistor operates at \( I_D = 0.4 \text{mA} \) and \( V_D = +0.5 \text{V} \). The NMOS transistor has \( V_t = 0.7 \text{V} \), \( \mu_n C_{ox} = 100 \ \mu \text{A/V}^2 \), \( L = 1 \ \mu \text{m} \), and \( W = 32 \ \mu \text{m} \). Neglect the channel-length modulation effect (i.e. assume that \( \lambda = 0 \)).

\[ R_D = ?, \quad R_S = ? \]
Example 5.5

Design the circuit to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_t=1$ V, $k'_nW/L=1$ mA/V$^2$.

$$r_{DS} = \frac{V_{DS}}{I_D}$$

$$V_{DD} = +5 \text{ V}$$

$$I_D$$

$$V_D = +0.1 \text{ V}$$
Example 5.6

Determine the voltages at all nodes and the currents through all branches. Let $V_{th} = 1$ V, $k' W/L = 1$ mA/V$^2$. Neglect the channel-length modulation effect.
5.3 MOSFET Circuit At DC

How about P-MOS?

(a)  
(b)  
(c)