Instructor: Oluwayomi Adamo - B 208  
Phone: 940-891-6874, oluwayomi.adamo@unt.edu  
Class Hours: Tue. 9:30 AM - 10:50 AM  
Office Hours: Tues. & Thurs. 4:00 PM - 5:00 PM

Teaching Assistant: TBD  
Office Hours: TBD

Prerequisite: Digital Logic Design (EENG 2710)

Textbook(s) and/or other required material  

Course Objective & Learning Outcome  
The main objective of the course is to facilitate the student in gaining a solid foundation in Digital Computer Organization and Design so that after completing the course students will able to:

- Understand essential components of a computer system  
- Understand Machine language such as MIPS and its addressing mechanisms  
- Understand Computer arithmetic and be able to design arithmetic logic units  
- Understand Computer performance parameters and benchmarks  
- Compare the performance of different computer systems  
- Understand processor datapath and control  
- Understand pipeline processing, pipeline control, data hazards & stalls, forwarding, Branch hazard  
- Understand Memory Hierarchy in a computer system, Caches, Measurement and improvement of cache performance, virtual memory  
- Understand types and characteristics of Buses, I/O devices and Interfaces  
- Understand multiprocessor based computer system and their performance

General Policy  
- Class attendance is mandatory. You will need to sign attendance sheet every class  
- It is strongly encouraged to get to know each other in the class. Discussions on course materials are allowed!  
- Everyone must turn in her/his own individual work. Simply copying other?s homework will be treated as a violation of academic honesty  
- It is the responsibility of students with certified disabilities to provide the instructor with appropriate documentation from the Dean of Students Office (see http://www.unt.edu/oda)  
- Please visit http://www.unt.edu/csrr/ for your rights and responsibilities

Grading Policy  
- 3 Tests – 60% (Test 1 - Feb 25, Test 2 - March 30, Test 3 - April 29)  
- Assignments – 20%  
- Quizzes – 10%  
- Project – 10%
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<tr>
<th></th>
<th>Topics (Tentative)</th>
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<tbody>
<tr>
<td>1</td>
<td>Computer Abstraction and Technology</td>
<td>2 classes</td>
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<tr>
<td>2</td>
<td>Computer Instructions</td>
<td>4 classes</td>
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<td>3</td>
<td>Arithmetic and Logic Unit</td>
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<td>4</td>
<td>Performance Analysis</td>
<td>3 classes</td>
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<td>5</td>
<td>Data Path and Control</td>
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<tr>
<td>6</td>
<td>Performance Enhancement with Pipelining</td>
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<tr>
<td>7</td>
<td>Memory Hierarchy and Virtual Memory Concepts</td>
<td>4 classes</td>
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<tr>
<td>8</td>
<td>Storage, Networks, and other Peripherals</td>
<td>3 classes</td>
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<tr>
<td>9</td>
<td>Multiprocessors and Applications</td>
<td>3 classes</td>
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